Publications

- Books and Book Chapters
  1. *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems, Edited by W. Rhee, The Institution of Engineering and Technology (IET),* June 2020.
  2. *Wireless Transceiver Circuits: System Perspectives and Design Aspects, Edited by W. Rhee and K. Iniewski, CRC Press*, Feb. 2015.

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  1. M. Ni, X. Wang, F. Li, W. Rhee, and Z. Wang, "A 13-Bit 2-GS/s time-interleaved ADC with improved correlation-based timing skew calibration strategy," accepted for *IEEE Trans. Circuits and Systems I*.
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- Invited Talks in International Conferences & Workshops
  1. W. Rhee, "PLL architectures, tradeoffs, and key application considerations," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2021. (online)
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  4. W. Rhee, "Energy-efficient proprietary transceivers for IoT and smartphone-based WPAN," *IEEE International Microwave Symposium (IMS) Workshop,* Philadelphia, Pennsylvania, June 2018.
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11. W. Rhee, “Phase-locked clocking and frequency synthesis - System perspectives tailored for IC designers,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015.
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14. W. Rhee, “Ultra-wideband technology for short-range communications,” *Solid-State Devices and Materials (SSDM)*, Tsukuba, Japan, Sept. 2014.
15. W. Rhee, “Frequency synthesizers: From basics to advanced bundle,” *IEEE Asian Solid-State Circuits Conference (A-SSCC) Tutorial*, Singapore, Nov. 2013.
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18. W. Rhee, “Frequency synthesizers and PLL,” *IEEE International Conference on Solid-State and Integrated-Circuit Technology (ICSICT) Tutorial*, Beijing, China, Oct. 2008.
19. W. Rhee, “Clocking frequencies and spectralizing clocks in SoC design,” *International SoC Design Conference (ISOCC) Tutorial*, Seoul, Korea, Oct. 2007.
20. W. Rhee, “Practical design aspects in fractional-*N* frequency synthesis,” *12th Workshop on Advances in Analog Circuit Design*, Graz, Austria, Apr. 2003.
21. D. Wilson, W. Rhee, and B. S. Song, “Integrated RF receiver front ends and frequency synthesizers for wireless,” *Emerging Technologies: Designing Low Power Digital Systems, Tutorial Workshops in IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 369-396, June, 1996.

- IEEE DL Talks & Webinar
  1. W. Rhee, "Phase-locked loops: System perspectives tailored for IC designers," *IEEE SSCS Webinar Series*, Nov. 2017.
  2. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in SSCS Kansai Chapter*, Dec. 2017.
  3. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in New South Wales Chapter*, Aug. 2017.
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  5. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in SSCS Atlanta Chapter*, Apr. 2017.

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- Patents
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- Ph.D. Thesis
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